REMARKS

Claims 1-8 remain in this application. Claims 1-8 are rejected. Claims 1-7 are amended herein to clarify the invention, and to broaden language as deemed appropriate. Other formal matters are attended to that were not addressed by the Examiner and accordingly are considered unrelated to substantive patentability issues.

ACKNOWLEDGMENT OF PRIORITY DOCUMENT

Applicant respectfully requests that the Examiner acknowledge receipt of the priority document filed in this application on April 4, 2001.

CLAIM REJECTIONS UNDER 35 U.S.C. § 102(b)

Claims 1, 2 and 5-8 are rejected under 35 U.S.C. § 102(b) as being anticipated by the Arita reference. Applicant herein respectfully traverses these rejections. "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" ***Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.***,

221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added). It is respectfully submitted that the cited reference is deficient with regard to the following.

Claim 1 is now amended to included selected subject matter of claim 2. It is respectfully submitted that claim 1 is clearly distinguished over the Arita reference by the following subject matter:

> the means for increasing the effective area including a lower semiconductor layer of the MIS structure being formed as one of a trench and a rugged portion such as to increase a surface area thereof of an interface of an insulator layer and the lower semiconductor layer of the MIS structure.

The Examiner indicates that Arita et al., esp. column 6 -7 and Fig. 1, teaches a semiconductor-type ferroelectric nonvolatile memory as recited in prior claim 2, and thus now recited in claim 1. It is respectfully submitted that the Examiner has misinterpreted the structure of the Arita et al. reference. Citing the Fig. 1 of Arita et al., Examiner alleges there is taught "a trench 38 formed in the semiconductor substrate 32" and that "the MIS structure 13 is formed in the trench 38." However, this is a mischaracterization of the Arita structure. Arita actually " teaches a via 38 formed in the BPSG, not in the semiconductor substrate 32. This is readily apparent from the following text of the Arita reference:

> MIS capacitor 13 comprises gate electrode 34, gate oxide 31 and semiconductor substrate 32. FET 12 and MIS 13 are covered by a

> standard interlayer dielectric ("ILD") 36, comprising a glasseous oxide, preferably a boron-doped phosphosilicate glass ("BPSG"). A via 38 from the top ILD 36 down to the surface of gate electrode 34 is filled with interconnect 39, also referred to herein the conventional term conductive plug 39. Col. 7, lines 29-36.

Accordingly, a lower layer of the MIS structure 13 in the Arita reference is the semiconductor substrate 32 which does not have a trench or rugged portion.

With regard to claim 5, the Examiner alleges that Arita et al., esp. column 7 and Fig. 1, teaches all structure of claim 5. It is stated that the region of source and drain of the MIS transistor are isolated by the trench." However, Arita states:

> Semiconductor substrate 32 comprises semiconductor material 22, source region 26, drain region 28, channel region 30, and gate oxide layer 31. FET 12 comprises source region 26, drain region 28, channel region 30, gate oxide layer 31 and gate electrode 34." Col. 7, lines 25-29.

Hence, since there is no trench between the source 26 and drain 28. Thus, said regions cannot be separated by a trench.

With regard to claim 6, Examiner alleges that Fig. 1 of Arita et al. teaches all structure of claim 6 including a rugged portion formed in the MIS structure.

However, the Arita reference fails to disclose any structure of the corresponding semiconductor layer 32 is rugged or rough. Likewise, with regard to claim 7, Arita fails to disclose MIM structure between the MFM structure and the MIS structure.

In view of the above, it is respectfully submitted that claims 1, 2 and 5-8 particularly describe and distinctly claim elements not disclosed in the cited reference. Therefore, reconsideration of the rejections of claims 1, 2 and 5-8 and their allowance are respectfully requested.

In accordance with MPEP 706.02(j), when a claim is rejected the Examiner should set forth "the relevant teachings of the prior art relied upon, preferable with reference to the relevant column or page number(s) and line number(s)." In order for the applicant to respond appropriately, it is respectfully requested that, in the event the pending claims are rejected based on the cited references, the Examiner set forth the relevant teachings in the cited references with reference to relevant column and line numbers or reference designators.

CLAIM REJECTIONS UNDER 35 U.S.C. §103(a)

Claims 3 and 4 are rejected as obvious over The Arita reference in view of the Matsuki reference under 35 U.S.C. §103(a). The applicant herein respectfully

traverses this rejection. For a rejection under 35 U.S.C. §103(a) to be sustained, the differences between the features of the combined references and the present invention must be obvious to one skilled in the art.

It is respectfully submitted that the proffered combination of references cannot render the rejected claims obvious because the secondary Matsuki reference does not provide the teaching noted above with respect to the anticipation rejection that is absent from the primary Arita reference. Thus, the combination of prior art references fails to teach or suggest all the claim limitations.

Furthermore, the Examiner alleges that Matsuki teaches means for increasing the effective area is gate structure of the MIS transistor formed on the inner surface of the trench. However, in Fig. 2 of Matsui, there is neither description of gate structure nor a trench formed in the semiconductor substrate. A contact hole 105 cannot correspond to a trench of the claimed invention; a contact plug 107 cannot correspond to a gate electrode of the claimed invention; and an insulating layer 103 cannot correspond to transistor structure (source, base and drain) of the claimed invention.